

FEATURES

- Dual supervisory circuits
- Supply voltage range of 2.7 V to 5.5 V
- Pretrimmed threshold options: 1.8 V, 2.5 V, 3.3 V, and 5 V
- Adjustable 0.6 V voltage reference
- Maximum supply current of 40 μ A
- 140 ms (minimum) reset timeout
- Watchdog timer with 1.6 sec (typical) timeout
- RESET valid from $V_{DD} \geq 1.1$ V
- Push-pull RESET and RESET outputs
- 8-lead, narrow body SOIC package
- Temperature range: -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

- Supervising DSPs/microcontrollers
- Industrial and portable equipment
- Wireless systems
- Notebook/desktop computers

GENERAL DESCRIPTION

The ADM13305 is a dual voltage supervisor designed to monitor two supplies and provide a reset signal to DSP and microprocessor-based systems.

There are five models available, all of which feature a combination of internally pretrimmed undervoltage threshold options for monitoring 1.8 V, 2.5 V, 3.3 V, and 5 V supplies. There is also an adjustable input option with an undervoltage threshold voltage of 0.6 V.

The ADM13305-18, ADM13305-25, and ADM13305-33 models have two internally fixed thresholds. The ADM13305-4 and ADM13305-5 offer one internally fixed threshold and one externally programmable threshold via a resistor string. See the Ordering Guide for a list of all available options.

During power-up, RESET is asserted when the supply voltage exceeds 1.1 V. The device then monitors the SENSEv input pins and holds the RESET output low as long as either of the SENSEv inputs remains below the rising threshold voltage, V_{IT+} .

Once the supplies monitored at the SENSEv inputs rise above their associated thresholds, the reset signal remains low for the reset timeout period before deasserting. Subsequently, if a voltage monitored by the SENSEv pins falls below its associated falling threshold, V_{IT-} , the RESET output asserts. The ADM13305 features both an active high RESET and an active low RESET output.

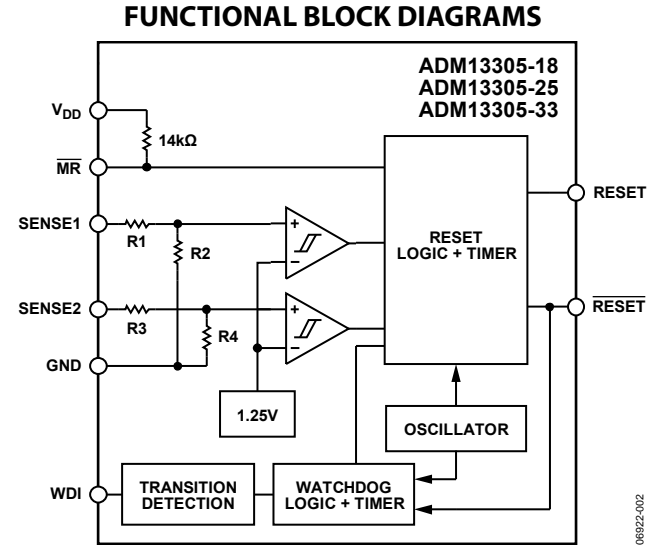


Figure 1.

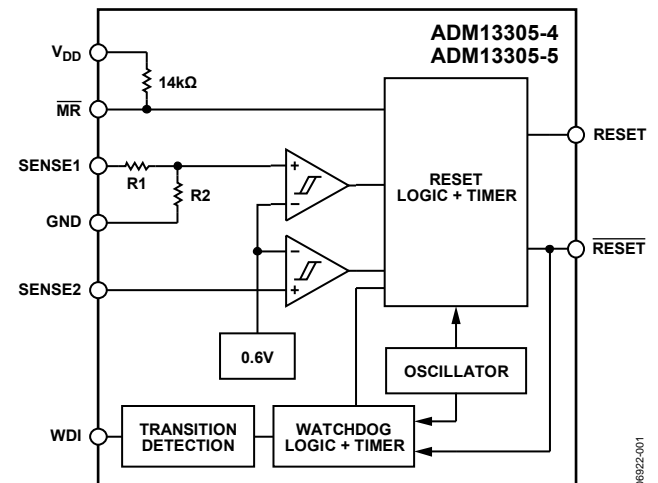


Figure 2.

As well as providing power-on reset signals, an on-chip watchdog timer can reset the microprocessor if it fails to strobe within the preset timeout period. A reset signal can also be asserted by an external push button through the manual reset input pin.

The ADM13305 is available in an 8-lead, narrow body SOIC package. The device operates over the extended industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise noted.

Table 1. ADM13305-18, ADM13305-25, and ADM13305-33

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING VOLTAGE RANGE, V_{DD}	2.7		5.5	V	
SUPPLY CURRENT, I_{DD}			40	μA	
INPUT CAPACITANCE, C_I		10		pF	$V_I = 0\text{ V to }V_{DD}$
RESET, $\overline{\text{RESET}}$ OUTPUT					
High Level Output Voltage, V_{OH}	$V_{DD} - 0.2$			V	$I_{OH} = -20\ \mu\text{A}$
	$V_{DD} - 0.4$			V	$I_{OH} = -2\ \text{mA}$, $V_{DD} = 3.3\ \text{V}$
	$V_{DD} - 0.4$			V	$I_{OH} = -3\ \text{mA}$, $V_{DD} = 5.5\ \text{V}$
Low Level Output Voltage, V_{OL}			0.2	V	$I_{OL} = 20\ \mu\text{A}$
			0.4	V	$I_{OL} = 2\ \text{mA}$, $V_{DD} = 3.3\ \text{V}$
			0.4	V	$I_{OL} = 3\ \text{mA}$, $V_{DD} = 5.5\ \text{V}$
Power-Up Reset Voltage ¹			0.4	V	$I_{OL} = 20\ \mu\text{A}$, $V_{DD} \geq 1.1\ \text{V}$
SENSE INPUTS					
Falling Threshold Voltage, V_{IT-}	1.64	1.68	1.72	V	$T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$
	2.20	2.25	2.30	V	$T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$
	2.86	2.93	3.00	V	$T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$
	4.46	4.55	4.64	V	$T_A = 0^{\circ}\text{C to }85^{\circ}\text{C}$
	1.64	1.68	1.73	V	$T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$
	2.20	2.25	2.32	V	$T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$
	2.86	2.93	3.02	V	$T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$
	4.46	4.55	4.67	V	$T_A = -40^{\circ}\text{C to }+85^{\circ}\text{C}$
Hysteresis at SENSEv Inputs, V_{HYS}		15		mV	$V_{IT-} = 1.68\ \text{V}$
		20		mV	$V_{IT-} = 2.25\ \text{V}$
		30		mV	$V_{IT-} = 2.93\ \text{V}$
		40		mV	$V_{IT-} = 4.55\ \text{V}$
WDI					
Average High Level Input Current, $I_{H(AV)}$		100	150	μA	$\text{WDI} = V_{DD} = 5.5\ \text{V}$
Average Low Level Input Current, $I_{L(AV)}$		-15	-20	μA	$\text{WDI} = 0\ \text{V}$, $V_{DD} = 5.5\ \text{V}$
INPUT VOLTAGE AT $\overline{\text{MR}}$ AND WDI					
High Level, V_{IH}	$0.7 \times V_{DD}$			V	
Low Level, V_{IL}			$0.3 \times V_{DD}$	V	
INPUT TRANSITION RISE AND FALL RATE AT $\overline{\text{MR}}$			50	ns/V	
HIGH LEVEL INPUT CURRENT, I_H					
WDI		120	170	μA	$\text{WDI} = V_{DD} = 5.5\ \text{V}$
$\overline{\text{MR}}$		-130	-180	μA	$\overline{\text{MR}} = 0.7 \times V_{DD}$, $V_{DD} = 5.5\ \text{V}$
SENSE1		5	8	μA	$\text{SENSE1} = V_{DD} = 5.5\ \text{V}$
SENSE2		6	9	μA	$\text{SENSE2} = V_{DD} = 5.5\ \text{V}$
LOW LEVEL INPUT CURRENT, I_L					
WDI		-120	-170	μA	$\text{WDI} = 0\ \text{V}$, $V_{DD} = 5.5\ \text{V}$
$\overline{\text{MR}}$		-430	-600	μA	$\overline{\text{MR}} = 0\ \text{V}$, $V_{DD} = 5.5\ \text{V}$
SENSEv	-1		+1	μA	$\text{SENSE1, SENSE2} = 0\ \text{V}$

¹ The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. t_r , $V_{DD} \geq 15\ \mu\text{s/V}$.

ADM13305

$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, unless otherwise noted.

Table 2. ADM13305-4 and ADM13305-5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING VOLTAGE RANGE, V_{DD}	2.7		5.5	V	
SUPPLY CURRENT, I_{DD}			40	μA	
INPUT CAPACITANCE, C_i		10		pF	$V_i = 0\text{ V to } V_{DD}$
RESET, $\overline{\text{RESET}}$ OUTPUT					
High-Level Output Voltage, V_{OH}	$V_{DD} - 0.2$			V	$I_{OH} = -20\ \mu\text{A}$
	$V_{DD} - 0.4$			V	$I_{OH} = -2\ \text{mA}$, $V_{DD} = 3.3\ \text{V}$
	$V_{DD} - 0.4$			V	$I_{OH} = -3\ \text{mA}$, $V_{DD} = 5.5\ \text{V}$
Low-Level Output Voltage, V_{OL}			0.2	V	$I_{OH} = 20\ \mu\text{A}$
			0.4	V	$I_{OH} = 2\ \text{mA}$, $V_{DD} = 3.3\ \text{V}$
			0.4	V	$I_{OH} = 3\ \text{mA}$, $V_{DD} = 5.5\ \text{V}$
Power-Up Reset Voltage ¹			0.4	V	$I_{OH} = 20\ \mu\text{A}$, $V_{DD} \geq 1.1\ \text{V}$
SENSEv INPUTS					
Falling Input Threshold Voltage, V_{IT-}	0.5952	0.6	0.6048	V	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$
	2.23	2.25	2.29	V	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$
	2.90	2.93	2.98	V	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$
Hysteresis at SENSEv Inputs, V_{HYS}		0		mV	$V_{IT-} = 0.6\ \text{V}$
		20		mV	$V_{IT-} = 2.25\ \text{V}$
		30		mV	$V_{IT-} = 2.93\ \text{V}$
WDI					
Average High Level Input Current, $I_{H(AV)}$		100	150	μA	$\text{WDI} = V_{DD} = 5.5\ \text{V}$
Average Low Level Input Current, $I_{L(AV)}$		-15	-20	μA	$\text{WDI} = 0\ \text{V}$, $V_{DD} = 5.5\ \text{V}$
INPUT VOLTAGE AT $\overline{\text{MR}}$ AND WDI					
High Level, V_{IH}	$0.7 \times V_{DD}$			V	
Low Level, V_{IL}			$0.3 \times V_{DD}$	V	
INPUT TRANSITION RISE AND FALL RATE AT $\overline{\text{MR}}$					
			50	ns/V	
HIGH LEVEL INPUT CURRENT, I_H					
WDI		120	170	μA	$\text{WDI} = V_{DD} = 5.5\ \text{V}$
$\overline{\text{MR}}$		-130	-180	μA	$\overline{\text{MR}} = 0.7 \times V_{DD}$, $V_{DD} = 5.5\ \text{V}$
SENSE1		5	8	μA	$\text{SENSE1} = V_{DD} = 5.5\ \text{V}$
SENSE2	-50		+50	nA	$\text{SENSE2} = V_{DD} = 5.5\ \text{V}$
LOW LEVEL INPUT CURRENT, I_L					
WDI		-120	-170	μA	$\text{WDI} = 0\ \text{V}$, $V_{DD} = 5.5\ \text{V}$
$\overline{\text{MR}}$		-430	-600	μA	$\overline{\text{MR}} = 0\ \text{V}$, $V_{DD} = 5.5\ \text{V}$
SENSEv	-1		+1	μA	$\text{SENSE1, SENSE2} = 0\ \text{V}$

¹ The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_r, V_{DD} \geq 15\ \mu\text{s/V}$.

TIMING REQUIREMENTS

$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $R_L = 1 \text{ M}\Omega$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$.

Table 3. ADM13305-18, ADM13305-25 and ADM13305-33

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PULSE WIDTH (t_w)					
SENSEv	6			μs	$V_{\text{SENSEvL}} = V_{\text{IT-}} - 0.3 \text{ V}$, $V_{\text{SENSEvH}} = V_{\text{IT+}} + 0.3 \text{ V}$
MR	100			ns	$V_{\text{IH}} = 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} = 0.3 \times V_{\text{DD}}$
WDI	100			ns	$V_{\text{IH}} = 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} = 0.3 \times V_{\text{DD}}$

Table 4. ADM13305-4 and ADM13305-5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PULSE WIDTH (t_w)					
SENSEv		30		μs	$V_{\text{SENSEvL}} = V_{\text{IT-}} - 0.3 \text{ V}$, $V_{\text{SENSEvH}} = V_{\text{IT+}} + 0.3 \text{ V}$
MR	100			ns	$V_{\text{IH}} = 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} = 0.3 \times V_{\text{DD}}$
WDI	100			ns	$V_{\text{IH}} = 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} = 0.3 \times V_{\text{DD}}$

SWITCHING CHARACTERISTICS

$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $R_L = 1 \text{ M}\Omega$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$.

Table 5. ADM13305-18, ADM13305-25 and ADM13305-33

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Watchdog Timeout (t_{OUT})	1.1	1.6	2.3	sec	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$
Delay Time (t_d)	140	200	280	ms	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$
Propagation Delay, High-to-Low, $\overline{\text{MR}}$ to RESET ¹ / $\overline{\text{RESET}}$ (t_{PHL})		200	500	ns	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $V_{\text{IH}} \geq 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} \geq 0.3 \times V_{\text{DD}}$
Propagation Delay, Low-to-High, $\overline{\text{MR}}$ to RESET/ $\overline{\text{RESET}}$ ¹ (t_{PLH})		200	500	ns	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $V_{\text{IH}} \geq 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} \geq 0.3 \times V_{\text{DD}}$
Propagation Delay, High-to-Low, SENSEv to RESET ¹ / $\overline{\text{RESET}}$ (t_{PHL})		1	5	μs	$V_{\text{IH}} = V_{\text{IT+}} + 0.3 \text{ V}$, $V_{\text{IL}} = V_{\text{IT-}} - 0.3 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$
Propagation Delay, Low-to-High, SENSEv to RESET/ $\overline{\text{RESET}}$ ¹ (t_{PLH})		1	5	μs	$V_{\text{IH}} = V_{\text{IT+}} + 0.3 \text{ V}$, $V_{\text{IL}} = V_{\text{IT-}} - 0.3 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$

¹ The reset timeout delay of 200 ms masks the propagation delay.

Table 6. ADM13305-4 and ADM13305-5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Watchdog Timeout (t_{OUT})	1.1	1.6	2.3	sec	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$
Delay Time (t_d)	140	200	280	ms	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$
Propagation Delay, High-to-Low, $\overline{\text{MR}}$ to RESET ¹ / $\overline{\text{RESET}}$ (t_{PHL})		200	500	ns	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $V_{\text{IH}} \geq 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} \geq 0.3 \times V_{\text{DD}}$
Propagation Delay, Low-to-High, $\overline{\text{MR}}$ to RESET/ $\overline{\text{RESET}}$ ¹ (t_{PLH})		200	500	ns	$V_{\text{I(SENSEv)}} \geq V_{\text{IT+}} + 0.2 \text{ V}$, $V_{\text{IH}} \geq 0.7 \times V_{\text{DD}}$, $V_{\text{IL}} \geq 0.3 \times V_{\text{DD}}$
Propagation Delay, High-to-Low, SENSEv to RESET ¹ / $\overline{\text{RESET}}$ (t_{PHL})		30		μs	$V_{\text{IH}} = V_{\text{IT+}} + 0.3 \text{ V}$, $V_{\text{IL}} = V_{\text{IT-}} - 0.3 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$
Propagation Delay, Low-to-High, SENSEv to RESET/ $\overline{\text{RESET}}$ ¹ (t_{PLH})		30		μs	$V_{\text{IH}} = V_{\text{IT+}} + 0.3 \text{ V}$, $V_{\text{IL}} = V_{\text{IT-}} - 0.3 \text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{\text{DD}}$

¹ The reset timeout delay of 200 ms masks the propagation delay.

FUNCTIONAL TRUTH TABLE**Table 7.**

MR	SENSE1 > V _{IT1}	SENSE2 > V _{IT2}	RESET	RESET
L	X ¹	X ¹	L	H
H	0	0	L	H
H	0	1	L	H
H	1	0	L	H
H	1	1	H	L

¹ X = don't care.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Supply Voltage Range, V_{DD}	-0.3 V to +6 V
\overline{MR} , \overline{WDI}	-0.3 V to $V_{DD} + 0.3$ V
SENSE1, SENSE2	$(V_{DD} + 0.3 \text{ V})V_{IT}/V_{REF}$
RESET, \overline{RESET}	-0.3 V to +6 V
Maximum Low Output Current	5 mA
Maximum High Output Current	-5 mA
Input Clamp Current ($V_i < 0 \text{ V}$, $V_i > V_{DD}$)	± 20 mA
Output Clamp Current ($V_o < 0 \text{ V}$, $V_o > V_{DD}$)	± 20 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 9.

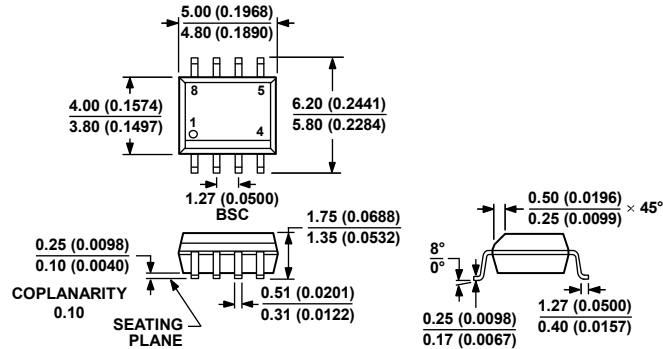
Package Type	θ_{JA}	Unit
8-Lead SOIC_N (R-8)	206	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 17. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

019407-A

ORDERING GUIDE

Model	Nominal Supervised Voltage		Threshold Voltage (Typical)		Temperature Range	Package Description	Package Option
	SENSE1	SENSE2	SENSE1	SENSE2			
ADM13305-18ARZ ¹	3.3 V	1.8 V	2.93 V	1.68 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-18ARZ-RL7 ¹	3.3 V	1.8 V	2.93 V	1.68 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-25ARZ ¹	3.3 V	2.5 V	2.93 V	2.25 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-25ARZ-RL7 ¹	3.3 V	2.5 V	2.93 V	2.25 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-33ARZ ¹	5 V	3.3 V	4.55 V	2.93 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-33ARZ-RL7 ¹	5 V	3.3 V	4.55 V	2.93 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-4ARZ ¹	3.3 V	Adjustable ²	2.93 V	0.6 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-4ARZ-RL7 ¹	3.3 V	Adjustable ²	2.93 V	0.6 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-5ARZ ¹	2.5 V	Adjustable ²	2.25 V	0.6 V	-40°C to +85°C	8-Lead SOIC_N	R-8
ADM13305-5ARZ-RL7 ¹	2.5 V	Adjustable ²	2.25 V	0.6 V	-40°C to +85°C	8-Lead SOIC_N	R-8

¹ Z = RoHS Compliant Part.

² 0.6 V adjustable. External resistor divider determines the actual sense voltage.